

HC540 OCTAL BUS BUFFER INVERTING (3-STATE)
HC541 OCTAL BUS BUFFER (3-STATE)

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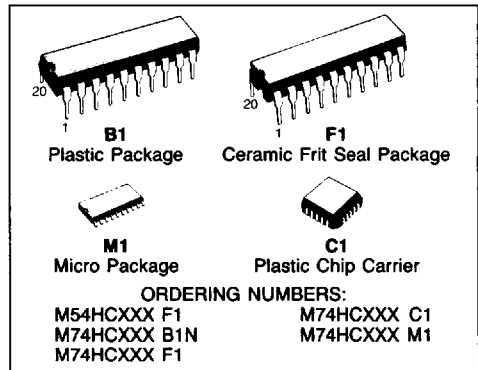
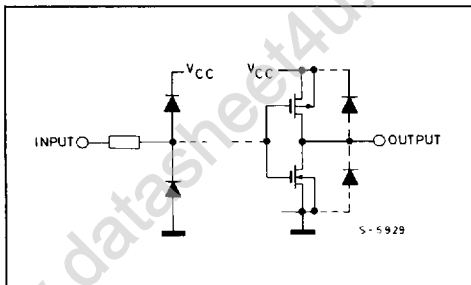
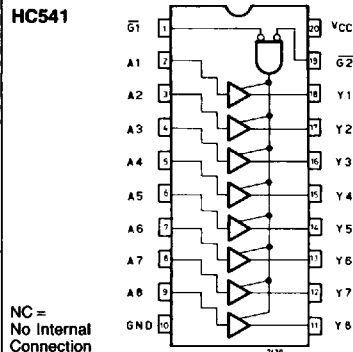
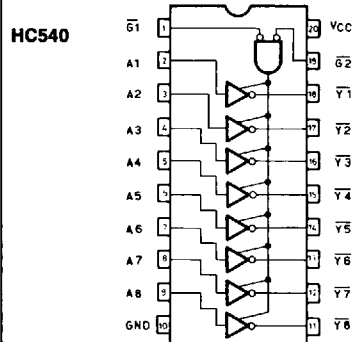
- **HIGH SPEED**
 $t_{PD} = 11 \text{ ns (TYP.) at } V_{CC} = 5\text{V}$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 15 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 6 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2\text{V to } 6\text{V}$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS540/541

DESCRIPTION

The M54/74HC540/541 are high speed CMOS OCTAL BUS BUFFERS (3-STATE) fabricated in silicon gate CMOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54/74HC540 is an inverting buffer and the M54/74HC541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input AND such that if either G1 or G2 are high, all eight outputs are in the high-impedance state.

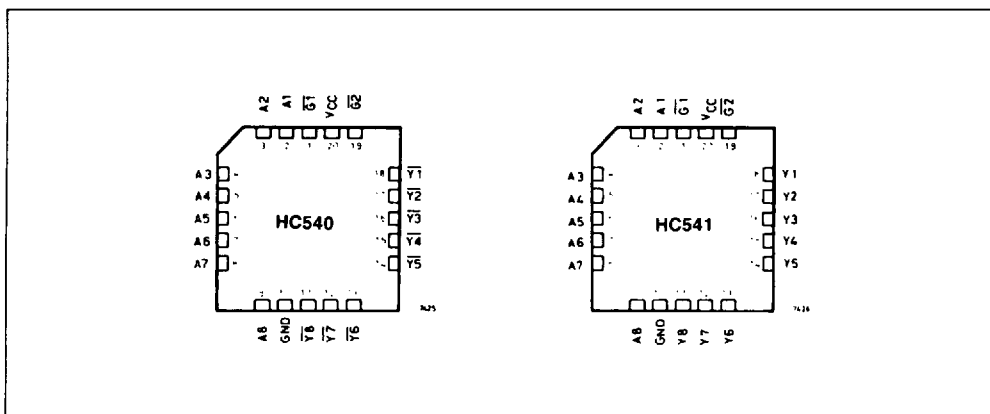
In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT**PIN CONNECTIONS (top view)**

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CHIP CARRIER



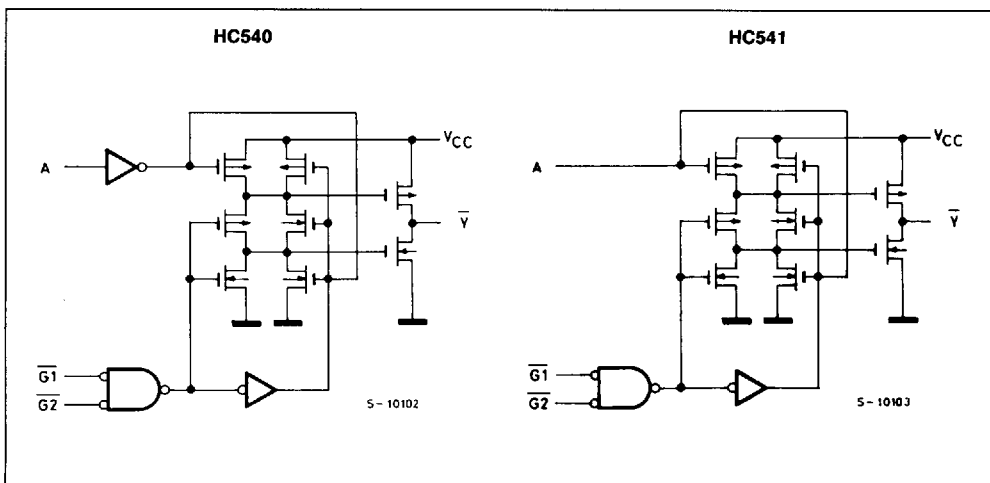
TRUTH TABLE

INPUTS			OUTPUT	
$\overline{G1}$	$\overline{G2}$	A_n	Y_n^*	\overline{Y}_n^*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: DON'T CARE Z: HIGH IMPEDANCE

*: Y_nHC541 \overline{Y}_nHC540

CIRCUIT DIAGRAM (Per Circuit)



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	2 to 6	V	
V _I	Input Voltage	0 to V _{CC}	V	
V _O	Output Voltage	0 to V _{CC}	V	
T _A	Operating Temperature	74HC Series 54HC Series	-40 to 85 -55 to 125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} { 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5	—	—	1.5	—	1.5	—	V	
		4.5		3.15	—	—	3.15	—	3.15	—		
		6.0		4.2	—	—	4.2	—	4.2	—		
V _{IL}	Low Level Input Voltage	2.0		—	—	0.5	—	0.5	—	0.5	V	
		4.5		—	—	1.35	—	1.35	—	1.35		
		6.0		—	—	1.8	—	1.8	—	1.8		
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH}		4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V _{IL}		4.18	4.31	—	4.13	—	4.10	—	
V _{OL}	Low Level Output Voltage	2.0	V _{IH}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5			V _{IL}	4.0 mA	—	0.17	0.26	—	0.33	
6.0	—	5.2 mA	—	0.18	0.26	—	0.33	—	0.40			

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DC SPECIFICATIONS (Continued)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND	—	—	±0.1	—	±1.0	—	±1.0	μA
I _{OZ}	3-State Output Off-State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND	—	—	±0.5	—	±5.0	—	±10	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND	—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0 4.5 6.0		— — —	25 7 6	60 12 10	— — —	75 15 13		90 18 15	ns
t _{PLH} t _{PHL}	Propagation Delay Time	2.0 4.5 6.0	HC540	— — —	52 13 11	105 21 18	— — —	130 26 22		160 32 27	ns
t _{PLH} t _{PHL}	Propagation Delay Time	2.0 4.5 6.0	HC541		56 14 12	15 23 20	— — —	145 29 25	— — —	135 35 30	ns
t _{PLZ} t _{PHZ}	3-State Output Enable	2.0 4.5 6.0	R _L = 1KΩ	— — —	72 18 15	145 29 25	— — —	180 36 31	— — —	220 44 38	ns
t _{PLZ} t _{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	R _L = 1KΩ	— — —	88 22 19	160 32 27	— — —	200 40 34	— — —	240 48 41	ns
C _{IN}	Input Capacitance			—	5	10	—	10		10	pF
C _{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C _{PD} (1)	Power Dissipation Capacitance		HC540	—	33	—	—	—	—	—	pF
			HC541	—	36	—	—	—	—	—	

Note (1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

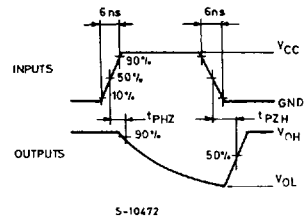
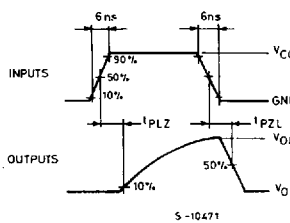
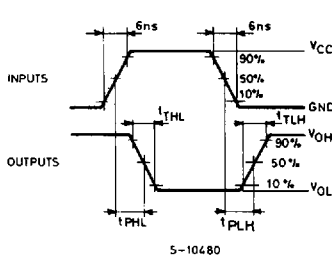
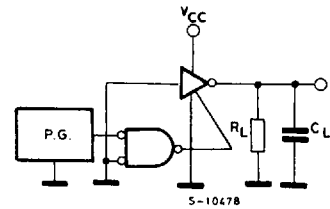
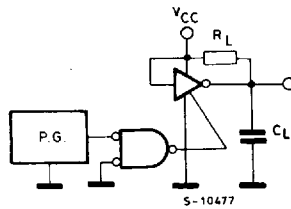
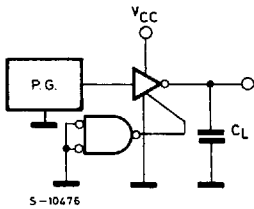
Average operating current can be obtained by the following equation.

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Gate).}$$

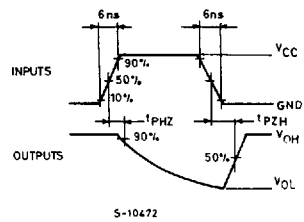
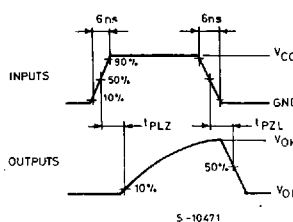
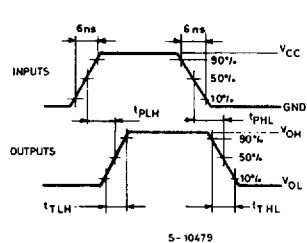
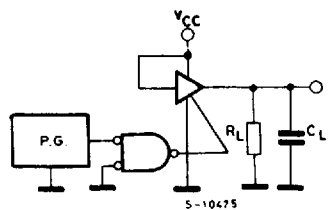
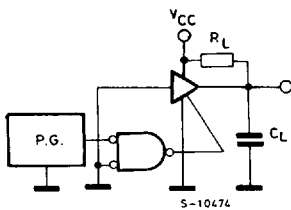
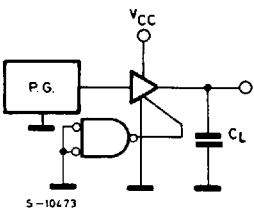
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SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

HC540



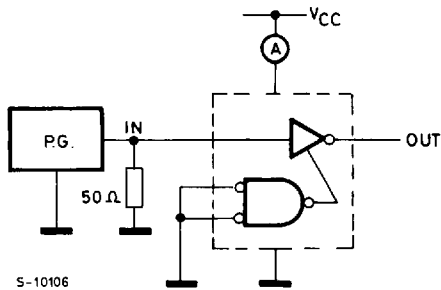
HC541



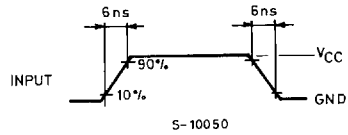
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TEST CIRCUIT I_{CC} (Opr.)

HC540



S-10106



THE OTHER INPUTS ARE CONNECTED V_{CC} LINE OR GND LINE.

TEST CIRCUIT OF THE HC541 IS THE SAME AS THIS